IN THE CLAIMS:

1. (Original) A variable gain amplifier circuit comprising:

a plurality of variable gain circuits;

a plurality of level detector circuits which detect signal levels at respective inputs of said plurality of variable gain circuits; and

a plurality of gain control circuits which separately control respective gains of said plurality of variable gain circuits,

wherein each of said plurality of gain control circuits determines a gain to be set therein, based on the signal level detected by one which is connected thereto of said plurality of level detector circuits and information about gain control received from a part or all of other gain control circuits existing in its preceding stage or stages.

2. (Original) The variable gain amplifier circuit according to claim 1,

wherein said plurality of level detector circuits are connected to said plurality of variable gain circuits, respectively, and

wherein said plurality of gain control circuits are connected to said plurality of level detector circuits, respectively.

3. (Original) The variable gain amplifier circuit according to claim 1, further comprising:

a plurality of filters separately connected to respective outputs of said plurality of variable gain amplifiers; and

a filtered attenuation evaluating circuit which evaluates the quantity of signal attenuation by said plurality of filters, based on the signal levels detected by said plurality of level detector circuits,

wherein each of said gain control circuits controls the gain of one which is connected thereto of said variable gain amplifiers, based on signal attenuation evaluated by said filtered attenuation evaluating circuit and the signal level detected and output by one which is connected thereto of said plurality of level detector circuits.

4. (Original) The variable gain amplifier circuit according to claim 1, further comprising:

a plurality of filters separately connected to respective outputs of said plurality of variable gain amplifiers;

an interference attenuation evaluating circuit which evaluates the quantity of attenuation of interference signals, based on the signal levels detected by said plurality of level detector circuits, taking advantage of idle mode duration; and

an interference attenuation retaining circuit which retains a value of attenuation evaluated by said interference attenuation evaluating circuit during a receiving mode,

wherein each of said gain control circuits controls the gain of one which is connected thereto of said variable gain amplifiers, based on information of the value of attenuation of interference signals retained during said receiving mode and the signal level detected and output by one which is connected thereto of said plurality of level detector circuits.

5. (Original) A receiver circuit comprising:

a variable gain low-noise amplifier which amplifies received high frequency signals;

a mixer which converts a signal output from said variable gain low-noise amplifier into an intermediate frequency signal;

a variable gain circuit which amplifies a signal output from the mixer;

a first level detector circuit which detects the signal level of said variable gain low-noise amplifier;

a first gain control circuit which controls the gain of said variable gain low-noise amplifier;

a second level detector circuit which detects the signal level of said variable gain circuit; and

a second gain control circuit which controls the gain of said variable gain circuit,

wherein said first gain control circuit controls the gain of said variable gain low-noise amplifier, based on the signal level detected by said first level detector circuit, and supplies information about the gain control to said second gain control circuit, and

wherein said second gain control circuit controls the gain of said variable gain circuit, based on the signal level detected by said second level detector circuit and said information about the gain control.

6. (Original) The receiver circuit according to claim 5,

wherein said variable gain circuit comprises one or a plurality of variable gain amplifiers and one or a plurality of filters,

wherein said second level detector circuit detects signal levels at respective inputs of said variable gain amplifiers, and

wherein said second gain control circuit controls the gain or gains of said one or plurality of variable gain amplifiers.

7. (Original) The receiver circuit according to claim 6,

wherein said first level detector circuit is connected to the inputs of said variable gain amplifiers.

8. (Original) The receiver circuit according to claim 5,

wherein said variable gain circuit comprises one or a plurality of variable gain amplifiers and one or a plurality of filters,

wherein said second level detector circuit detects signal levels at respective outputs of said variable gain amplifiers, and

wherein said second gain control circuit controls respective gains of said variable gain amplifiers.

9. (Original) The receiver circuit according to claim 5, further comprising:

a plurality of filters separately connected to respective outputs of said plurality of variable gain amplifiers; and

a filtered attenuation evaluating circuit which evaluates the quantity of signal attenuation by said plurality of filters, based on the signal levels detected by said plurality of level detector circuits,

wherein said gain control circuit controls the respective gains of said variable gain amplifiers, based on signal attenuation evaluated by said filtered attenuation evaluating circuit and the signal levels detected and output by said plurality of level detector circuits.

10. (Original) The receiver circuit according to claim 5, further comprising:

a plurality of filters separately connected to respective outputs of said plurality of variable gain amplifiers;

an interference attenuation evaluating circuit which evaluates the quantity of attenuation of interference signals, based on the signal levels detected by said plurality of level detector circuits, taking advantage of idle mode duration; and

an interference attenuation retaining circuit which retains a value of attenuation evaluated by said interference attenuation evaluating circuit during a receiving mode,

wherein said gain control circuit controls the respective gains of said variable gain amplifiers, based on information of the value of attenuation of interference signals retained during said receiving mode and the signal levels detected and output by said plurality of level detector circuits.

11. and 12. (Cancel)